Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 86565

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2021.

Third Semester

Electronics and Communication Engineering

EC 1201 – DIGITAL ELECTRONICS

(Regulations 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Prove the Boolean theorems $x + x = x$, $x \cdot x = x$.

2. What are don't care minterms? State the use of don't care minterms.

3. What is tristate logic? What are the demerits?

4. State the features of Bipolar logic families.

5. Give the circuit and truth table of Half-adder.

6. Define Multiplexer.

7. Give significance of priority encoder.

8. Distinguish between EPROM and EEPROM.

9. Enumerate the types of ROMs.

10. Compare PAL and PLA devices.

PART B — (5 × 16 = 80 marks)

11. (a) (i) With suitable examples, explain the conversion of standard forms to canonical forms of Boolean expression. (5)

(ii) Implement the given Boolean function $F = xy + x'y' + y'z$ using with NAND and inverter gates. (6)

(iii) Verify, whether or not Exclusive OR operation is commutative and associative. (5)

Or

(b) (i) Show the five variable Karnaugh map and explain the minimization technique. (8)

(ii) Minimize the given Boolean function using Karnaugh map.

$F(A, B, C, D) = \sum(0, 2, 3, 5, 7, 8, 9, 10, 11, 13, 15)$. (8)

12. (a) (i) Draw a CMOS NAND gate and explain its operation. List the characteristics of CMOS Logic family. (10)

(ii) Draw a tristate TTL gate and explain its operation. (6)

Or

(b) (i) Compare the features of TTL, ECL and HTL families. (10)

(ii) Enumerate the precautionary measures to be considered while handling CMOS device. (6)

13. (a) (i) Design and implement 8 × 1 multiplexer using suitable gates. (8)

(ii) Design 3 bit parity generator and checker circuit. (8)

Or

(b) (i) Design and implement full subtractor using suitable gates. (8)

(ii) Design the logic diagram of Magnitude comparator to compare two binary variables A and B accompanied by 3 bits each. (8)

14. (a) (i) Design a synchronous decade counter to count in the following sequence. 1, 0, 2, 3, 4, 8, 7,6, 5. (8)

(ii) What is sequential circuit? Explain S-R and J K flip flop. (8)

Or

(b) (i) Draw and explain 4-bit synchronous Up / Down counter. (8)

(ii) Design a serial 2's complementer with a shaft register and a flip-flop. The binary number is shifter out from one side and its 2's complement shifted into the other side of the shift register. (8)

15. (a) Discuss the programmable Logic Array (PTA) in detail.

Or

(b) Write an elaborate note on :

(i) Static RAM cell. (8)

(ii) Field programmable Gate Arrays (FPGA). (8)

———————